

ABSTRACT OF THE DISCLOSURE

A frequency synthesizing circuit is provided. The frequency synthesizing circuit includes a frequency multiplying circuit and a phase-locked loop, wherein the frequency multiplying circuit can convert a reference signal having a low frequency into a high
5 frequency signal for being a reference signal of the phase-locked loop, so that the loop bandwidth of the phase-locked loop can be increased to reduce jitter of the output signal. The present invention utilizes the delay-locked loop to generate multiphase output signals that equivalently divide a cycle of the reference signal for achieving a frequency multiplying through cooperating with a phase synthesizer. Through double frequency
10 multiplying functions of the delay loop and the phase locked loop, a phase error accumulation caused by the single frequency multiplying of the conventional phase-locked loop with narrow loop bandwidth can be reduced. Furthermore, the frequency multiplying can be adjusted by synthesizing different phases of delay-locked loop and the divider coefficient of the phase-locked loop.

【Main portions of representative symbols】

- 14 Phase frequency detector
- 16 Charge pump filter
- 18 Voltage-control oscillator
- 20 Divider
- 41 Frequency multiplying circuit
- 42 Phase-locked loop
- 51 Delay circuit
- 52 Delay circuit
- 53 Delay circuit
- 54 Delay circuit
- 55 Phase detector
- 56 Loop filter
- 57 Phase synthesizer
- 58 Phase frequency detector
- 59 Loop filter
- 60 Voltage control oscillator
- 61 Divider
- 62 Reference signal
- 63 Control signal
- 65 High frequency signal
- 66 Output signal
- 67 Output signal
- 68 Output signal
- 69 DC (Direct Current) voltage
- 70 Output phase
- 71 Signal

81 Digital logic selector

82 Multiplexer

83 Phase synthesizer